Listing of Claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled).

6. (Currently amended) A method for fabricating a metal alloy interconnect in a semiconductor device, comprising:

defining a metal alloy interconnect boundary profile on a substrate material;

subjecting the substrate material to a first wet process for fabricating an intermediate layer of the metal alloy interconnect conforming to the boundary profile;

subjecting the substrate material having the intermediate layer to a second wet process for fabricating a main layer of the metal alloy interconnect containing a primary metal,

wherein the intermediate layer has a relatively higher concentration of a secondary metal than the main layer and the first wet process is controlled by using a relatively high bias voltage to create the relatively higher concentration of the secondary metal.

7. (Currently amended) The method of claim 6 wherein the first and second wet processes include[[s]] at least one electro-chemical plating process.

8. (Currently amended) The method of claim 6 wherein the first and second wet processes include[[s]] at least one electroless plating process.

9. (Canceled).

10. (Original) The method of claim 6 wherein the second wet process is controlled by using a relatively low bias voltage to maintain a relatively low concentration of the secondary metal.

11. (Original) The method of claim 6 wherein the first and second wet processes are further enhanced by adjusting plating temperatures in the processes, thereby adjusting a thermal budget for fabricating the metal alloy interconnect.

12. (Original) The method of claim 6 wherein the primary metal is Cu.

13. (Currently amended) The method of claim 6 further comprising fabricating a seed layer before fabricating the intermediate layer wherein ~~so that~~ the seed layer is underneath the intermediate layer.

14. (Original) The method of claim 13 wherein the seed layer has pure primary metal.

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (New) A method for fabricating an interconnect in a semiconductor device, the method comprising:

defining an interconnect boundary profile, comprising vias or trenches, on a substrate material;

plating a first layer of interconnect along the interconnect boundary profile, the first layer of interconnect comprising a primary metal with one or more impurities; and

plating a second layer of interconnect over the first layer of interconnect, the second layer of interconnect comprising the primary metal with one or more impurities, wherein the second layer of interconnect is thicker than the first layer of interconnect and the second layer of interconnect has a lower electrical resistance than the first layer of interconnect.

22. (New) The method of claim 21, wherein the second layer of interconnect has a lower concentration of impurities than the first layer of interconnect.

23. (New) The method of claim 21, wherein the plating steps include at least one electro-chemical plating process.

24. (New) The method of claim 21, wherein the plating steps include at least one electroless plating process.

25. (New) The method of claim 21, wherein the plating processes are further enhanced by adjusting plating temperatures in the processes, thereby adjusting a thermal budget for fabricating the metal alloy interconnect.

26. (New) The method of claim 21, wherein the primary metal is Cu.

27. (New) The method of claim 21, further comprising plating a seed layer on the substrate before plating the first layer of interconnect, wherein the seed layer is underneath the first layer of interconnect.

28. (New) The method of claim 27, wherein the seed layer comprises pure primary metal.

29. (New) The method of claim 21, wherein the first layer of interconnect substantially fills the vias for improved electromigration resistance of the vias.

30. (New) The method of claim 29, wherein the plating processes include at least one electro-chemical plating process.

31. (New) The method of claim 29, wherein the plating processes include at least one electroless plating process.

32. (New) The method of claim 29, wherein the plating processes are further enhanced by adjusting plating temperatures in the processes, thereby adjusting a thermal budget for plating the interconnect layers.

33. (New) The method of claim 29, wherein the primary metal is Cu.

34. (New) The method of claim 29, further comprising plating a seed layer on the substrate before plating the first layer of interconnect wherein the seed layer is underneath the first layer of interconnect.

35. (New) The method of claim 34, wherein the seed layer comprises pure primary metal.

36. (New) A method for fabricating an interconnect in a semiconductor device, the method comprising:

defining an interconnect boundary profile on a substrate material;

plating a layer of the interconnect on the substrate material using an electro-chemical plating process, the interconnect layer comprising a primary metal and an impurity metal, wherein a plating bias voltage is applied to the substrate material and the interconnect layer conforms to the boundary profile; and

continuously varying the plating bias voltage during the plating step to achieve a complex series of layers within the interconnect wherein a gradient of concentration of the impurity metal is formed within the interconnect layer, wherein the concentration of the impurity metal in the complex series of layers is relatively higher near the substrate than further away from the substrate.

37. (New) The method of claim 36, wherein the interconnect layer contains copper.

38. (New) The method of claim 36, further comprising plating a seed layer on the substrate before plating the layer of interconnect wherein the seed layer is underneath the interconnect layer.

39. (New) The method of claim 38, wherein the seed layer comprises pure copper.